IN THE CLAIMS

Cancel claims 1-11 and 14-30, amend claims 12, 13 and 35-37, and add new claims 38-43 as follows:

1-11. (Canceled).

12. (Currently Amended) A semiconductor integrated circuit device ~~as claimed in Claim 9~~, comprising:

a PMOS transistor formed in a N-type well;

an NMOS transistor formed in a P-type well;

first-layer metal line layers;

second-layer metal line layers;

a plurality of contact holes for connecting said first-layer metal line layers to gate electrodes and diffusion layers of said PMOS and NMOS transistors; and

through holes for connecting said first-layer metal line layers to said second-layer metal line layers, wherein

a potential of said N-type well and a potential of said P-type well are controlled independently of each other;

lines for obtaining the potentials of said N-type and P-type wells includes said first-layer metal line layers, electrical conductors formed inside said contact holes, or

said electrical conductors formed inside said contact holes and said first-layer metal line layers; and

said second-layer metal line layers wire a power supply potential and a ground potential;

said electrical conductors formed inside said contact holes and said first-layer metal line layers are formed with tungsten as a main constituent; and

said second-layer metal line layers are formed with copper as a main constituent wherein

a dynamic random access memory is integrated on an identical chip on which said semiconductor integrated circuit device is integrated, said dynamic random access memory using memory cells each of which includes one capacitance element and one transistor; and

bit lines of said dynamic random access memory are formed said first-layer metal line layers.

13. (Currently Amended) A semiconductor integrated circuit device ~~as claimed in Claim 12~~, comprising:

a PMOS transistor formed in a N-type well;

an NMOS transistor formed in a P-type well;

first-layer metal line layers;

second-layer metal line layers;

a plurality of contact holes for connecting said first-layer metal line layers to gate electrodes and diffusion layers of said PMOS and NMOS transistors; and

through holes for connecting said first-layer metal line layers to said second-layer metal line layers, wherein

a potential of said N-type well and a potential of said P-type well are controlled independently of each other;

lines for obtaining the potentials of said N-type and P-type wells includes said first-layer metal line layers, electrical conductors formed inside said contact holes, or said electrical conductors formed inside said contact holes and said first-layer metal line layers; and

said second-layer metal line layers wire a power supply potential and a ground potential;

said electrical conductors formed inside said contact holes and said first-layer metal line layers are formed with tungsten as a main constituent; and

said second-layer metal line layers are formed with copper as a main constituent wherein

a dynamic random access memory is integrated on an identical chip on which said semiconductor integrated circuit device is integrated, said dynamic random access memory using memory cells each of which includes one capacitance element and one transistor; and

bit lines of said dynamic random access memory are formed said first-layer metal line layers, wherein said capacitance element is formed at a height between a height of said first-layer metal line layer and a height of said second-layer metal line layer.

14-30. (Canceled).

31. (Original) A semiconductor integrated circuit device, comprising:

a MIS transistor formed in a substrate;

a memory cell for storing data;

a first metal line layer formed on said substrate; and

a second metal line layer formed on said first metal line layer, wherein

at least a part of a power supply line connected to a source/drain channel in said MIS transistor is constituted by said second metal line layer;

at least a part of a well potential line for controlling a well potential of said MIS transistor is constituted by said first metal line layer; and

at least a part of a bit line for transmitting an input or output data signal to said memory cell is constituted by said first metal line layer.

32. (Original) A semiconductor integrated circuit device, comprising:

a MIS transistor formed in a substrate;

a memory cell for storing data;

a first line layer a main constituent of which is tungsten; and

a second line layer a main constituent of which is copper, wherein

at least a part of a power supply line connected to a source/drain channel in said MIS transistor is constituted by said second line layer;

at least a part of a well potential line for controlling a well potential of said MIS transistor is constituted by said first line layer; and

at least a part of a bit line for transmitting an input or output data signal to said memory cell is constituted by said first line layer.

33. (Original) A semiconductor integrated circuit device, comprising:

a MIS transistor formed in a substrate;

a memory cell for storing data;

a first metal line layer formed on said substrate, a main constituent of said first metal line layer being tungsten; and

a second metal line layer formed on said first metal line layer, a main constituent of said second metal line being copper, wherein

at least a part of a power supply line connected to a source/drain channel in said MIS transistor is constituted by said second metal line layer; and

at least a part of a bit line for transmitting an input or output data signal to said memory cell is constituted by said first metal line layer.

34. (Original) A semiconductor integrated circuit device as claimed in Claim 33, wherein at least a part of a well potential line for controlling a well potential of said MIS transistor is constituted by said first metal line layer.

35. (Currently Amended) A semiconductor integrated circuit device as claimed in claim 33 ~~or 34~~, wherein

said memory cell is a DRAM cell; and

a capacitor of said DRAM cell is located between said first metal line layer and said second metal line layer.

36. (Currently Amended) A semiconductor integrated circuit device as claimed in ~~any one of~~ claim~~s~~ 33 ~~to 35~~,

wherein a gate electrode layer is located between said substrate and said first metal line layer.

37. (Amended) A semiconductor integrated circuit device as claimed in ~~any one of~~ claim~~s~~ 33 ~~to 36~~, further comprising:

a contact hole for connecting two of said substrate, said first metal line layer, said second metal line layer and said gate electrode layer which are selected as a first connection object and a second connection object, wherein

when an X-Y plane is assumed on a surface of said substrate, projection onto said X-Y plane of a contact surface of said first connection object and said contact hole has a portion at which said projection does not overlap with a mapping onto said X-Y plane of a contact surface of said second connection object and said contact.

38. (New) A semiconductor integrated circuit device as claimed in claim 34, wherein

said memory cell is a DRAM cell; and

a capacitor of said DRAM cell is located between said first metal line layer and said second metal line layer.

39. (New) A semiconductor integrated circuit device as claimed in claim 34, wherein a gate electrode layer is located between said substrate and said first metal line layer.

40. (New) A semiconductor integrated circuit device as claimed in claim 35, wherein a gate electrode layer is located between said substrate and said first metal line layer.

41. (New) A semiconductor integrated circuit device as claimed in claim 34, further comprising:

a contact hole for connecting two of said substrate, said first metal line layer, said second metal line layer and said gate electrode layer which are selected as a first connection object and a second connection object, wherein

when an X-Y plane is assumed on a surface of said substrate, projection onto said X-Y plane of a contact surface of said first connection object and said contact hole has a

portion at which said projection does not overlap with a mapping onto said X-Y plane of a contact surface of said second connection object and said contact.

42. (New) A semiconductor integrated circuit device as claimed in claim 35, further comprising:

a contact hole for connecting two of said substrate, said first metal line layer, said second metal line layer and said gate electrode layer which are selected as a first connection object and a second connection object, wherein

when an X-Y plane is assumed on a surface of said substrate, projection onto said X-Y plane of a contact surface of said first connection object and said contact hole has a portion at which said projection does not overlap with a mapping onto said X-Y plane of a contact surface of said second connection object and said contact.

43. (New) A semiconductor integrated circuit device as claimed in claim 36, further comprising:

a contact hole for connecting two of said substrate, said first metal line layer, said second metal line layer and said gate electrode layer which are selected as a first connection object and a second connection object, wherein

when an X-Y plane is assumed on a surface of said substrate, projection onto said X-Y plane of a contact surface of said first connection object and said contact hole has a portion at which said projection does not overlap with a mapping onto said X-Y plane of a contact surface of said second connection object and said contact.